Surface and Interface States in Topological Crystalline Insulators

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A new class of 3D topological materials - topological crystalline insulators (TCI) - has been proposed theoretically[1] and discovered experimentally by angle- and spin-resolved photoemission spectroscopy (ARPES) as well as scanning tunneling spectroscopy (STS) techniques. In contrast to topological materials based on Bi and Sb chalcogenides, in TCIs the topological protection of surface electronic states is warranted not by time reversal symmetry but by mirror-plane crystalline symmetry[1]. So far, the TCI states have been found in IV-VI narrow-gap semiconductors $Pb_{1-x}Sn_xTe$ (x=0.4-1) and $Pb_{1-x}Sn_xSe$ (x=0.18-0.4) for (001) and (111) crystal surfaces. These materials possess direct bulk energy gap at four L-points of the Brillouin zone and undergo a band inversion at specific Sn content and temperature. In the inverted bands regime one observes topological in-gap states forming 4 pairs of Dirac cones located across the edge of the (001) surface Brillouin zone. By lowering the crystal symmetry, via strain or crystal distortion, one can modify the energy spectrum of topological states as observed in $Pb_{1-x}Sn_xSe$ (001) by STS (in Landau quantization regime)[2] and ARPES experiments[3] that revealed the gap opening in energy spectrum of Dirac surface states.

Recently, the topological states were also observed for (001) surface of SnTe crystal in experimental studies of Shubnikov - de Haas and de Haas - van Alphen quantum oscillations[4]. By varying the angle between external magnetic field and the crystal we observed simultaneous contributions from neighboring (001) facets of the bulk crystal, thus demonstrating how the TCI topological states wrap the bulk of the crystal[4].

New concepts involving TCI materials, e.g. the idea of topological transistor, rely on layered heterostructures and the effects of strain, hybridization or size quantization on topological properties. It requires understanding of the topological states at realistic interfaces (with atomic steps or other defects) facing vacuum or buried within trivial semiconductor multilayer. The unique electronic properties of atomic steps were recently demonstrated with STM/STS technique revealing the 1D channels of high density electronic states located along the odd-monolayer-high atomic steps at (001) surface of $Pb_{1-x}Sn_xSe$[5]. By in-situ controlled capping of the TCI surface of $Pb_{0.7}Sn_{0.3}Se$ bulk crystal with an ultrathin topologically trivial layer of PbSe followed by ARPES studies we demonstrated the robustness of Dirac cones at $Pb_{1-x}Sn_xSe$/PbSe interface and the important role of atomic steps. Forming sufficiently short period lateral structure these steps may induce an oscillatory collapse of the pair of split Dirac cones into a single one.[6]

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